

10Gb/s SFP Optical Transceiver Module

SPP5100LR-GL

(10GBASE-LR, 1310nm DFB-LD, PIN-PD)

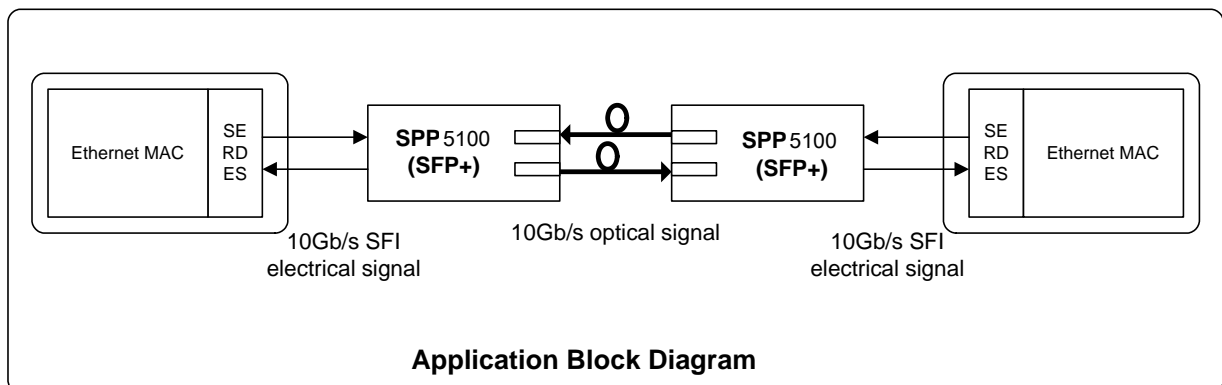
Features

- ◆ 10Gb/s Serial Optical Interface
 - High quality and reliability optical device and sub-assemblies
 - 1310nm DFB laser for up to 10km over Single Mode Fiber
 - High sensitivity PIN photodiode and TIA
- ◆ SFP+ MSA Compliant
 - Easy supply management for hot pluggability
 - Duplex LC Receptacle
 - SFP Mechanical Interface for easy removal
 - SFI High Speed Electrical Interface
 - 2-wire interface for management and diagnostic monitor
 - Tx_Disable and Rx_LOS functions
- ◆ Protocol
 - IEEE802.3ae 10 Gigabit Ethernet
 - LAN PHY/WAN PHY
- ◆ Power Supply
 - Single 3.3V power supply
 - Low power consumption
- ◆ RoHS6 compliant.



Applications

- ◆ 10GE Ethernet switches and routers
- ◆ 10GE Storage
- ◆ Inter Rack Connection
- ◆ Other high speed data connections



1. General Description

The SPP5100LR-GL is a very compact 10Gb/s optical transceiver module for serial optical communication applications at 10Gb/s. The SPP5100LR-GL converts a 10Gb/s serial electrical data stream to 10Gb/s optical output signal and a 10Gb/s optical input signal to 10Gb/s serial electrical data streams. The high speed 10Gb/s electrical interface is fully compliant with SFI specification.

The SPP5100LR-GL is designed for Ethernet LAN (10.3Gb/s) and WAN (9.95Gb/s) applications. The high performance 1310nm DFB-LD transmitter and high sensitivity PIN receiver provide superior performance for Ethernet applications at up to 10km links.

The fully SFP compliant form factor provides hot pluggability, easy optical port upgrades and low EMI emission.

Table 1. Fiber compliance

SFP+ type	Wavelength [nm]	Cable Type	Core Size (micron)	Modal Bandwidth [MHz/km]	Cable distance
10GB-LR	1310	SMF	G.652	--	10km

2. Functional Description

The SPP5100LR-GL contains a duplex LC connector for the optical interface and a 20-pin connector for the electrical interface. Figure 2.1 shows the functional block diagram of SPP5100LR-GL SFP Transceiver.

Transmitter Operation

The transceiver module receives 10Gb/s electrical data and transmits the data as an optical signal.

The transmitter output can be turned off by Tx disable signal, TX_DIS pin. When TX_DIS is asserted High, Transmitter is turned off.

Receiver Operation

The received optical signal is converted to serial electrical data signal.

The RX_LOS signal indicates insufficient optical power for reliable signal reception at the receiver.

Management Interface

A 2-wire interface (SCL, SDA) is used for serial ID, digital diagnostics and other control /monitor functions.

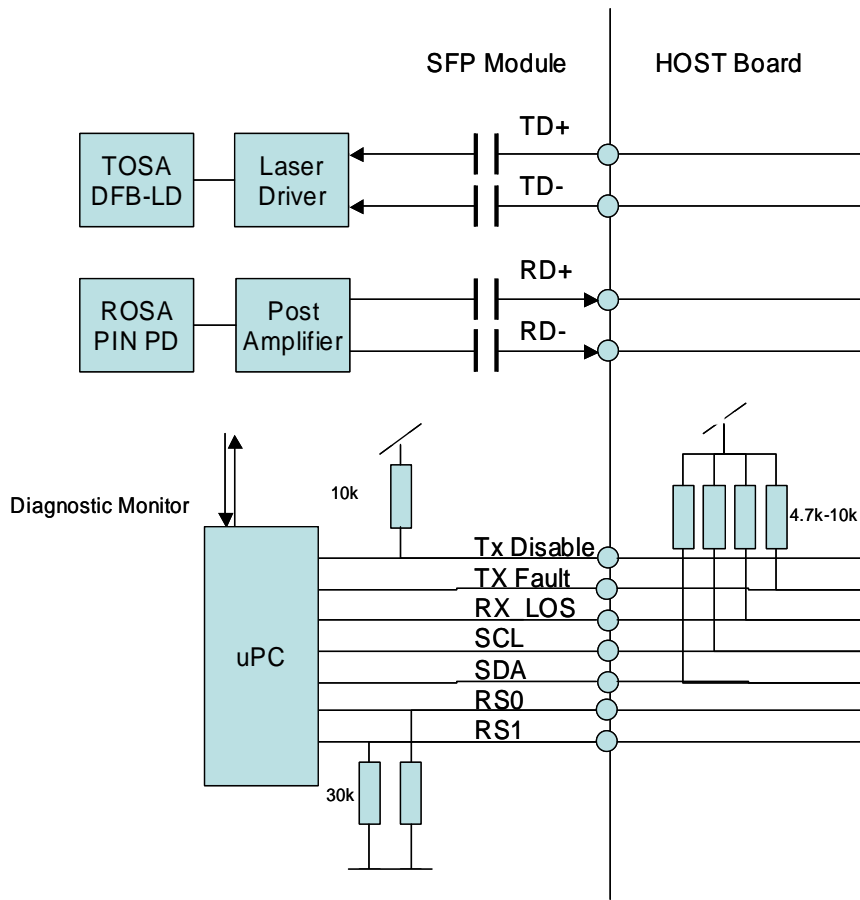


Figure 2.1. Functional Block Diagram

3. Package Dimensions

Figure 3.1. shows the package dimensions of SPP5100LR-GL. SPP5100LR-GL is designed to be compliant with SFP MSA specification. Package dimensions are specified in SFF-8432.

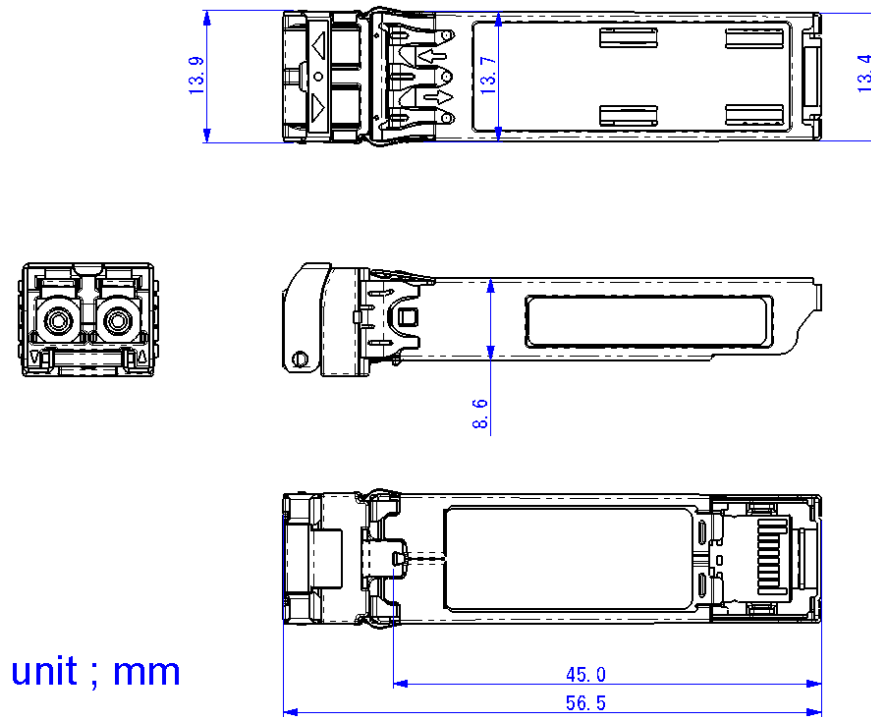


Figure 3.1. Package dimensions

4. Pin Assignment and Pin Description

4.1. SFP Transceiver Electrical Pad Layout

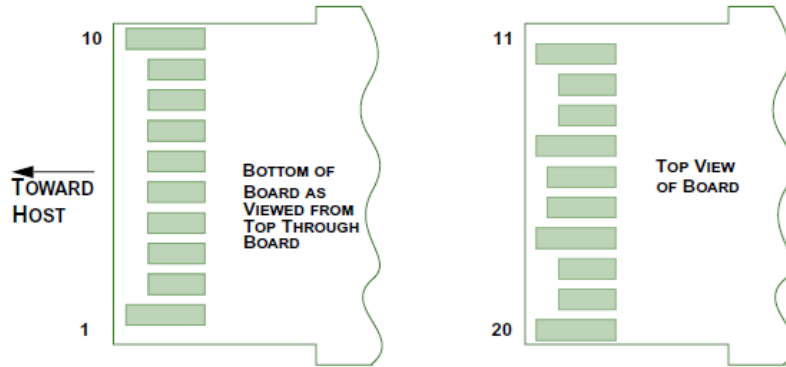


Figure 4.1. SFP Transceiver Electrical Pad Layout

4.2. Host PCB SFP Pinout

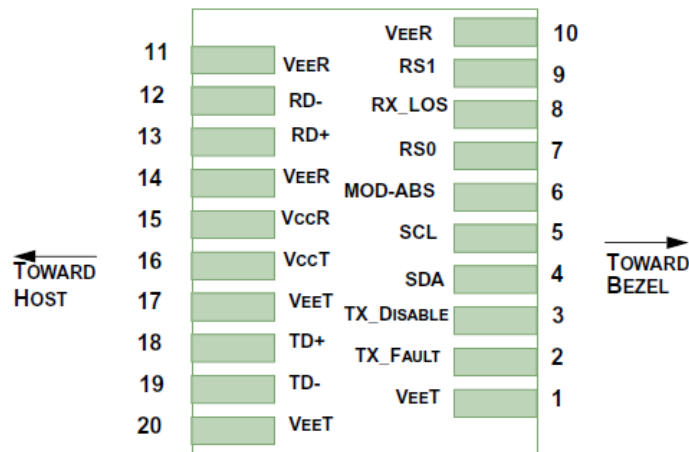


Figure 4.2. Host PCB SFP Pinout

4.3. Pin Descriptions

Table 4.3. Pin Description

Pin#	Name	Logic	Description	Power Sequence Order	Note
1	VeeT		Module Transmitter Ground	1 st	1
2	Tx_Fault	LVTTL-O	Module Transmitter Fault	3 rd	2
3	Tx_Disable	LVTTL-I	Transmitter Disable, Turns off transmitter laser output	3 rd	3
4	SDA	LVTTL-I/O	2 Wire Serial Interface Data Line (Same as MOD-DEF2 as defined in the INF-8074i)	3 rd	
5	SCL	LVTTL-I/O	2 Wire Serial Interface Data Line (Same as MOD-DEF1 as defined in the INF-8074i)	3 rd	
6	MOD_ABS		Module Absent, connected to VeeT or VeeR in the module	3 rd	2
7	RS0	LVTTL-I	Rate Select 0 (not functional for 10GE type)	3 rd	
8	RX_LOS	LVTTL-O	Receiver Loss of Signal Indication	3 rd	2
9	RS1	LVTTL-I	Rate Select 1 (not functional for 10GE type)	3 rd	
10	VeeR		Module Receiver Ground	1 st	1
11	VeeR		Module Receiver Ground	1 st	1
12	RD-	CML-O	Receiver Inverted Data Output	3 rd	
13	RD+	CML-O	Receiver Non-Inverted Data Output	3 rd	
14	VeeR		Module Receiver Ground	1 st	1
15	VccR		Module Receiver 3.3V Supply	2 nd	
16	VccT		Module Transmitter 3.3V Supply	2 nd	
17	VeeT		Module Transmitter Ground	1 st	1
18	TD+	CML-I	Transmitter Non-Inverted Data Input	3 rd	
19	TD-	CML-I	Transmitter Inverted Data Input	3 rd	
20	VeeT		Module Transmitter Ground	1 st	1

Note

- 1: Module ground pins are isolated from the module case and chassis ground within the module.
- 2: Shall be pulled up with 4.7k to 10k ohm to a voltage between 3.15V and 3.45V on the host board.
- 3: Shall be pulled up with 4.7k to 10k ohm to VccT in the module.

5. Absolute Maximum Ratings and Recommended Operating Conditions

Table 5.1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-40	85	degC	
Relative Humidity (non-condensation)	RH	-	85	%	
Operating Case Temperature	Topc	0	70	degC	
Supply Voltage	VccR/VccT	-0.5	3.6	V	
Voltage on LVTTL Input	Vilvttl	-0.5	VCC3+0.5	V	
LVTTL Output Current	Iolvttl	-	15	mA	
Voltage on Open Collector Output	Voco	0	6	V	
Receiver Input Optical Power(Average)	Mip	-	1.5	dBm	

Table 5.2. Recommended Operating Conditions and Supply Requirements

Parameter	Symbol	Min	Max	Unit	Note
Operating Case Temperature	Topc	0	70	degC	
Relative Humidity(non-condensing)	Rhop	-	85	%	
Power Supply Voltage	VccR/VccT	3.135	3.465	V	
Total Power Consumption	Pd	-	1.0	W	

6. Electrical Interface

6.1. High Speed Electrical Interface

SFI Application Reference model

Figure 6.1.1. shows the high speed electrical interface (SFI) compliance points.

SFI electrical interface is specified for each compliance point in the SFP MSA specification.

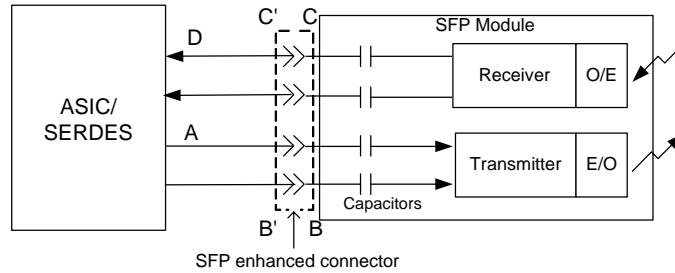


Figure 6.1.1. SFI Application Reference Model

SFI Module Transmitter Input Electrical Interface Specification at B' and Calibrated B''

Table 6.1.1. SFI Transmitter Input Electrical Specification at B'

Parameter B'	Symbol	Condition	Min	Typ.	Max.	Unit
Single Ended Output Voltage Tolerance		Referenced to VeeT	-0.3		4.0	V
AC common Input S-parameter			15			mV
Differential Input S-parameter (note 1)	SDD11	0.01-1GHz			-12	dB
		1-11.1GHz			Note 2	dB
Reflected Differential to Common Mode Conversion (note 3)	SCD11	0.01-11.1GHz			-10	dB

Note 1. Reference differential impedance is 100 ohm

2. Return Loss given by quation $SDD11(dB) = -12.9 + 0.9 * (f/1e9)$, with f in GHz

3. Common mode refernce impedance is 25 ohm

Table 6.1.2. SFI Transmitter Input Electrical Specification at B''

Parameter B''	Symbol	Condition	Min	Typ.	Max.	Unit
AC Common Mode Voltage		Note 1			15	MV
Total Jitter	TJ	Note 1		0.28		UIpp
Data Dependant Jitter	DDJ			0.10		UIpp
Pulse Width Shrinkage Jitter	DDPWS			0.055		UIpp
Uncorrelated Jitter	UJ	Note 2		0.023		UIrms
Eye Mask Figure 6.1.2	X1			0.14		UI
	X2				0.35	UI
	Y1			90		mV
	Y2				350	mV

Note 1. Re The tester is not expected to generate this common mode voltage however its output must not exceed this value.

2. It is not possible to have the worst UJ and DDJ simultaneously and meet the TJ specifications if the UJ is all Gaussian.

SFI Module Receiver Output Electrical Interface Specification at C'

Table 6.1.3. SFI Receiver Output Electrical Specification at C'

Parameter – C'	Symbol	Conditions	Min	Typ	Max	Units
Crosstalk source rise/fall time (20% to 80%)	Tr, Tf	Note 1		34		ps
Crosstalk Source Amplitude Differential (p-p)		Note 2		700		mV
Termination Mismatch at 1 MHz	ΔZ_M				5	%
Single Ended Output Voltage Tolerance			-0.3		4.0	V
Output AC Common Mode Voltage					7.5	mV (RMS)
Differential Output S-parameter (Note 3)	SDD22	0.01-1GHz			-12	dB
		1-11.1GHz			Note 4	dB
Common Mode Output Reflection Coefficient (Note 5)	SCC22	0.01-2.5GHz			-6	dB
		2.5-11.1GHz			-3	dB

Note1 : Measured with OMA test pattern. Use of five 1's and four 0's sequence in the PRBS 9 is an acceptable alternative.

- 2 : For dRNx compliance test condition. Crosstalk is not used for dRN.
- 3 : Reference differential impedance is 100 ohm.
- 4 : Differential Output S-parameter given by equation $SDD11(dB) = -12.9 + 0.9 \cdot (f/1e9)$, with f in GHz.
- 5 : Common mode reference impedance is 25 ohm.

Table 6.1.4. SFP+ Limiting Output Jitter and Eye Mask Specification at C'

Parameter – C'	Symbol	Conditions	Min	Typ	Max	Units
Output rise/fall time (20% to 80%)	Tr, Tf	Note 1	28			ps
Total Jitter	TJ	Note 2			0.70	UIpp
Deterministic Jitter	DJ				0.42	UIpp
Eye Mask Figure 6.1.3	X1				0.35	UI
	Y1		150			mV
	Y2				425	mV

Note1 : Measured at B' with Host Compliance Board and Module Compliance Board pair and with OMA test pattern. Use of five 1's and four 0's sequence in the PRBS 9 is an acceptable alternative.

2 : The data pattern for the total jitter measurement is one of IEEE 802.3 CL52.9 Pattern 1, Pattern 3, or valid 64B/66B data traffic.

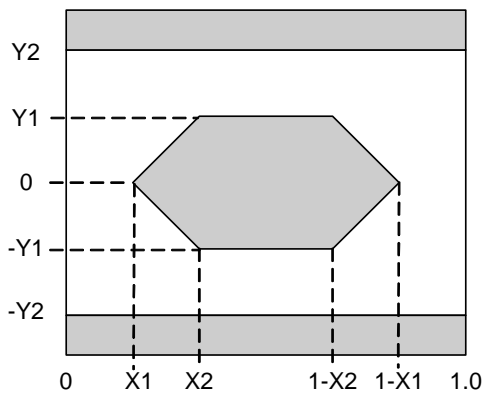


Figure 6.1.2.
Transmitter Input Eye Mask

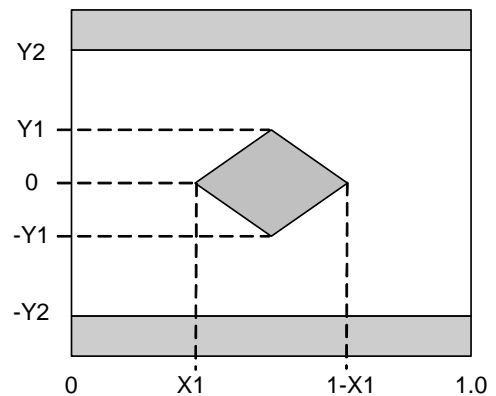


Figure 6.1.3.
Receiver Output Eye Mask

6.2. Low speed Electrical Interface

SPP5100LR-GL low speed interface is based on 2-wire interface. Management memory map is based on SFF-8472.

2-wire Electrical Specifications

Parameter	Symbol	Min	Max	Unit
Host 2-wire Vcc	Vcc_host	3.14	3.46	V
SCL and SDA	V _{OL}	0.0	0.40	V
	V _{OH}	Vcc_host-0.5	Vcc_host+0.3	V
SCL and SDA	V _{IL}	-0.3	VccT*0.3	V
	V _{IH}	VccT*0.7	VccT+0.5	V
Input current on the SCL and SDA contacts		-10	10	uA
Capacitance on SCL and SDA I/O contact			14	pF

2-wire Timing Specifications

Parameter	Symbol	Min	Max	Unit
Clock Frequency	f _{SCL}	0	400	kHz
Clock Pulse Width Low	t _{LOW}	1.3		us
Clock Pulse Width High	t _{HIGH}	0.6		us
Time bus free before new transmission can start	t _{BUF}	20		us
START Hold Time	t _{HD, STA}	0.6		us
START Set-up Time	t _{SU, STA}	0.6		us
Data In Hold Time	t _{HD, DAT}	0		us
Data In Set-up Time	t _{SU, DAT}	0.1		us
Input Rise Time (100kHz)	t _{R, 100}		1000	ns
Input Rise Time (400kHz)	t _{R, 400}		300	ns
Input Fall Time (100kHz)	t _{F, 100}		300	ns
Input Fall Time (400kHz)	t _{F, 400}		300	ns
STOP Set-up Time	t _{SU, STO}	0.6		us
Serial Interface Clock Holdoff “Clock Stretching”	t _{clock_hold}		500	us

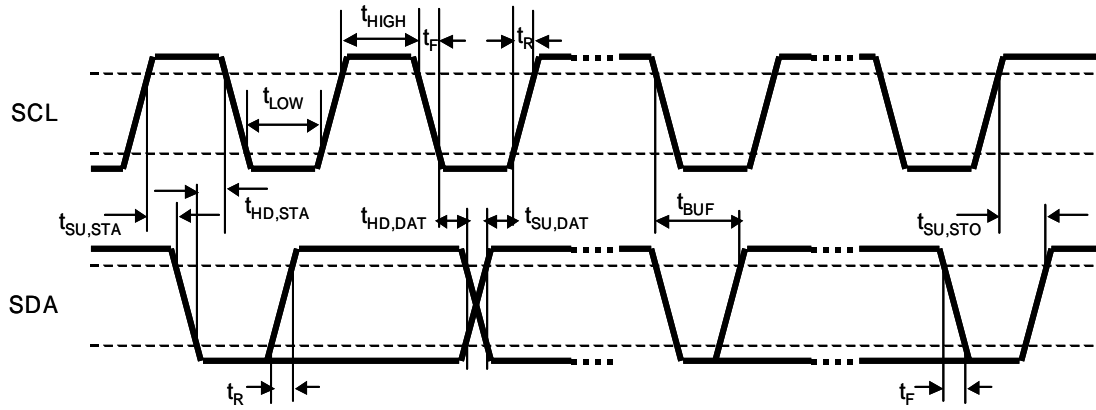


Figure 6.2.1. SFP+ Timing Diagram

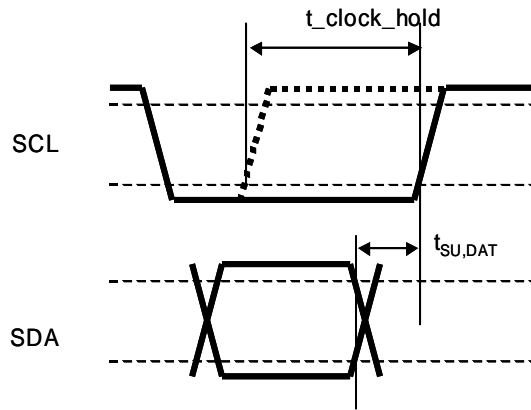


Figure 6.2.1. Detail of Clock Stretching

7. Optical Interface

Optical Interfaces of SPP5100LR-GL are defined in the IEEE802.3ae(10GBASE-LR).

Optical Transmitter

Parameter	Symbol	Min	Typ	Max	Unit
Signaling Speed (LAN PHY) (WAN PHY)		-	10.3125 9.95328		Gb/s
Signaling speed variation from nominal (max)		-100		+100	ppm
Center wavelength		1260		1355	nm
Side Mode Suppression Ratio	SMSR	30			dB
Average launched power	Pave	-8.2		+0.5	dBm
OMA	Poma	-5.2			dBm
OMA-TDP		-6.2			dBm
Transmitter and dispersion penalty	DP			3.2	dB
Average launch power of Tx OFF	Pave_off			-30	dBm
Extinction ratio	ER	3.5			dB
RIN OMA	RIN			-128	dB/Hz
Optical Return Loss Tolerance	ORLT			12	dB
Eye mask(X1,X2,X3,Y1,Y2,Y3)		(0.25, 0.40, 0.45, 0.25, 0.28, 0.40) Note 1			

Note 1: Refer to Figure 7.1.

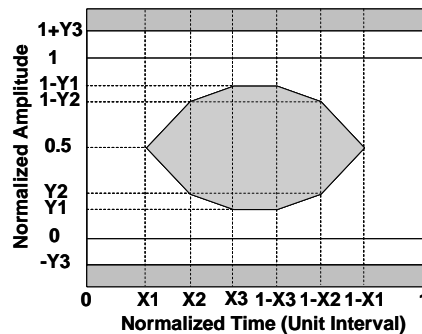


Figure.7.1. Transmission eye mask definition

Optical Receiver

Parameter	Symbol	Min	Typ	Max	Unit
Wavelength		1260		1355	nm
Signaling Speed (LAN PHY)			10.3125		Gb/s
Signaling Speed (WAN PHY)			9.95328		Gb/s
Signaling speed variation from nominal (max)		-100		+100	ppm
Average receiver power		-14.4		+0.5	dBm
Receiver sensitivity in OMA				-12.6	dBm
Receiver Reflectance				-12	dB
Stressed receiver sensitivity in OMA (Note 2)				-10.3	dBm
Vertical eye closure penalty		2.2			dB
Stressed ey jitter		0.3			UIpp
Receive electrical 3dB upper cutoff frequency				12.3	GHz

Note 1 : Receiver sensitivity is informative. Stressed receiver sensitivity shall be measured with conformance test signal for BER=10⁻¹².

Note 2 : The stressed sensitivity value in the table are for system level BER measurements which include the effects of CDR circuit.

8. Electrical and Optical I/O Signal Relationship

Table.8.1. TX_DIS vs. Optical Output Power

TX_DIS	Optical Output Power
Low ($V_{IL}=-0.3$ to $0.8V$)	Enabled
High ($V_{IH}=2.0$ to $VCC3+0.3V$)	Disabled ($<-30dBm$)

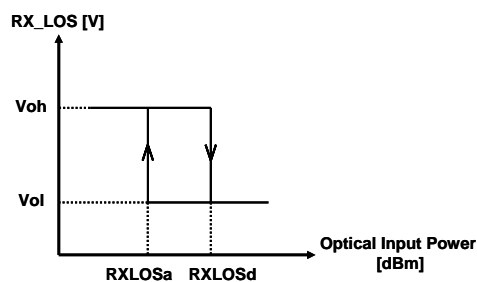


Figure.8.1. Optical Input Power vs. RX_LOS

9. User Interface

9.1. SFP Mechanical Interface

SFP Mechanical Interface is specified in the SFF-8432. Also, bail latch system is adequate for the particular specification.

9.2. Management Interface

SFP 2-Wire Serial Interface Protocol

SFP 2-wire serial interface is specified in the SFF-8472.

The SFP 2-wire serial interface is used for serial ID, digital diagnostics, and certain control functions. The 2-wire serial interface is mandatory for all SFP modules.

The 2-wire serial interface address of the SFP module is A0h and A2h. In order to access to a specific module on the 2-wire serial bus, the SFP has a MOD_ABS (module absent pin). This pin, which is pulled down in the module, must be held low to notify a module installation and to allow communication over 2-wire serial interface.

SFP Management Interface

SFP Managed interface is specified in the SFF-8472.

The Figure 9.2. shows the structure of the memory map. The normal 256 Byte address space is divided into lower and upper blocks of 128 Bytes. The lower block of 128 Byte is

always directly available and is used for the diagnostics and control functions that must be accessed repeatedly. Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. The upper address space tables are used for less frequently accessed functions and control space for future standards definition.

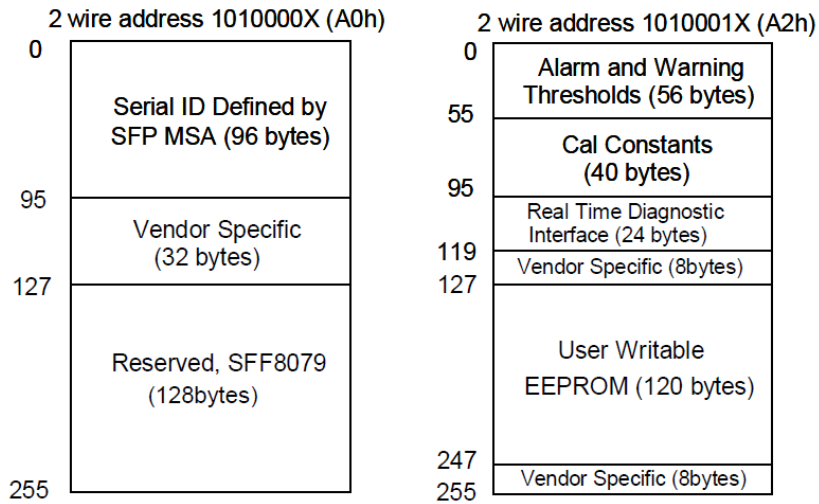


Figure 9.1. 2-wire Serial Interface Memory Map

9.3. Serial ID Memory Map (Data Field – Address A0h)

Address	Size (Bytes)	Name	Hex	ASC	Description	Address	Size (Bytes)	Name	Hex	ASC	Description		
0	1	Identifier	03		SFP module	64	2	Options	00		Power Class 1,		
1	1	Ext.Identifier	04		Serial ID module	65			1A	limit Receiver Output			
2	1	Connector	07		LC Connector						TxDisable, TxFault,		
3	1		20		10GE BASE-LR						LOS implemented		
4	8	Transceiver	00			66	1	BR_max	00				
5			00			67	1	BR_min	00				
6			00			68			xx				
7			00			69			xx				
8			00			70			xx				
9			00			71			xx				
10			00			72			xx				
11			1	Encoding	06		64B66B	73			xx		
12	1	BR, Nominal	67		10.3Gbps	74			xx				
13	1	Rate Identifier	00		unspecified	75			xx				
14	1	Length(9um, km)	0A		10km	76	16	Vendor SN	xx				
15	1	Length(9um)	64		10km	77			xx				
16	1	Length(50um)	00		not support MMF	78			xx				
17	1	Length(62.5um)	00		not support MMF	79			xx				
18	1	Length(Copper)	00		not support copper	80			xx				
19	1	Length(OM3)	00		not support MMF	81			xx				
20	16	Vendor name	53	S		82			xx				
21			75	u		83			xx				
22			6D	m		84	xx					Year code	
23			69	i		85	xx						
24			74	t		86	xx					Month code	
25			6F	o		87	xx						
26			6D	m		88	xx					Day code	
27			6F	o		89	xx						
28			45	E		90	xx					LOT code	
29			6C	l		91	xx						
30			65	e		92	68					68	Internal cal., Average Power
31			63	c		93	F0						Alarm/Warning flags, Soft
32			74	t									TxDisable, Soft TxFault,
33			72	r									Soft RxLOS implemented
34			69	i									Rev.10.0
35			63	c									Check Code *3
36	1	Channel Spacing	00			94	1	SFF-8472 Compliance	03				
37			00			95	1	CC_EXT	xx				
38	3	Vendor OUI	00			96-127	32	Vendor Specific	00				
39			5F			128-255	128	Reserved	00				
40	16	Vendor PN	53	S									
41			50	P									
42			50	P									
43			35	5									
44			31	1									
45			30	0									
46			30	0									
47			4C	L									
48			52	R									
49			2D	-									
50			47	G									
51			4C	L									
52			20										
53			20										
54			20										
55			20										
56	4	Vendor rev	41	A	*1								
57			20										
58			20										
59			20										
60	2	Wavelength	05										
61			1E										
62	1	DWDM Wavelength	00										
63	1	CC BASE	4B		Check Code *2								

*1 : Revision level for part number provided by vendor (ASCII). Variable
 *2 : Checksum of Add.0 to 62
 *3 : Checksum of Add.64 to 94

Note 1.The guaranteed +/- range of transmitter output wavelength under all normal operating conditions.

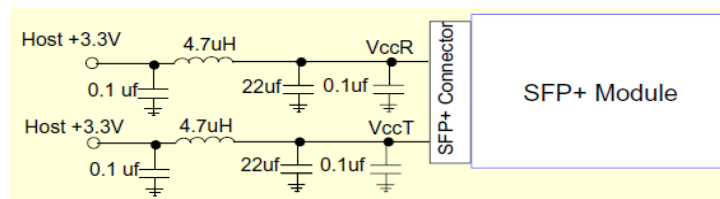


Figure 9.2. Supply Filter

9.4. Alarm/Warming threshold

A2h address	Meaning	Unit	SPP5100LR-GL
0-1	Temperature High Alarm	deg	75
2-3	Temperature Low Alarm	deg	-5
4-5	Temperature High Warning	deg	70
6-7	Temperature Low Warning	deg	0
8-9	Voltage High Alarm	V	3.63
10-11	Voltage Low Alarm	V	2.97
12-13	Voltage High Warning	V	3.465
14-15	Voltage Low Warning	V	3.135
16-17	Tx Bias High Alarm	mA	102
18-19	Tx Bias Low Alarm	mA	22
20-21	Tx Bias High Warning	mA	90
22-23	Tx Bias Low Warning	mA	29
24-25	Tx Power High Alarm	dBm	3.5
26-27	Tx Power Low Alarm	dBm	-12.2
28-29	Tx Power High Warning	dBm	0.5
30-31	Tx Power Low Warning	dBm	-8.2
32-33	Rx Power High Alarm	dBm	3.5
34-35	Rx Power Low Alarm	dBm	-18.4
36-37	Rx Power High Warning	dBm	0.5
38-39	Rx Power Low Warning	dBm	-14.4

Note. Alarm /Warming flag is linked to TxFault by default setting.

10. RoHS COMPLIANCY

Compliance versus requirements contained inside the following reference document is guaranteed: "Directive 2002/95/EC of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment" from official journal of European Union (European Parliament and of the Council). This product is Compliant at RoHS-6/6 level and contains no leaded solders.

11. Qualification Testing

SPP5100LR-GL 10Gb/s transceiver is qualified to Sumitomo Electric Industries internal design and manufacturing standards. Telecordia GR-468-CORE reliability test standards, using methods per MIL-STD-883 for mechanical integrity, endurance, moisture, flammability and ESD thresholds, are followed.

12. Laser Safety Information

SPP5100LR-GL transceiver uses a semiconductor laser system that is classified as Class 1 laser products per the Laser Safety requirements of FDA/CDRH, 21 CFR1040.10 and 1040.11. These products have also been tested and certified as Class 1 laser products per IEC 60825-1:2001 International standards.

Caution

If this product is used under conditions not recommended in the specification or is used with unauthorized revision, the classification for laser product safety is invalid. Reclassify the product at your responsibility and take appropriate safety measures.

13. Electromagnetic Compatibility

EMI (Emission)

SPP5100LR-GL is designed to meet FCC Class B limits for emissions and noise immunity per CENELEC EN50 081 and 082 specifications.

RF Immunity

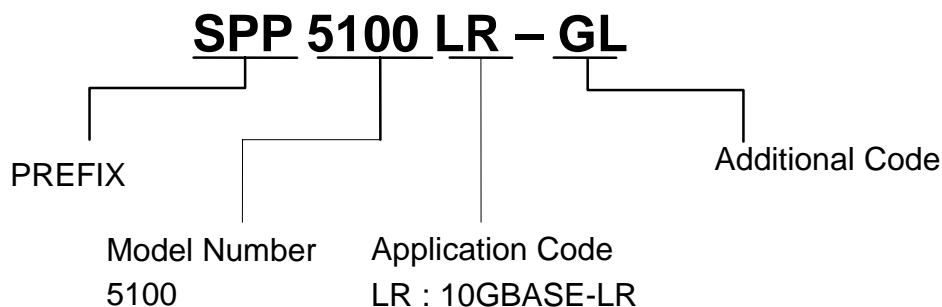
SPP5100LR-GL has an immunity to operate when tested in accordance with IEC 61000-4-3 (80- 1000MHz, Test Level 3) and GR-1089.

Electrostatic Discharge (ESD) Immunity

SPP5100LR-GL has an immunity against direct and indirect ESD when tested accordance with IEC 61000-4-2.

14. Ordering Information

14.1 Part Numbering System



14.3. Ordering Number Code

Table 14-1. SPP5100LR Application Code

P/N	Distance	Fiber	E/O	O/E	ITU-T G.691	Telecordia GR-253	IEEE 802.3ae
SPP5100LR-GL	10km	SMF	1310nm DFB	PIN	-	-	10GBASE-LR/LW

14.4. Firmware version

This product contains the firmware inside. Sumitomo Electric may upgrade the firmware version without advance notice as far as such would be upper compatible. When customer should prefer to have the current firmware version, Sumitomo Electric will accommodate such request and will assign customized part number for this purpose.

14.5. 2-wire Serial Interface

If the serial clock(SCL) is more than 100kHz, the SCL is held in line low (clock stretching) during an 2-WIRE SERIAL INTERFACE read or white operation.

15. Label information



16. Contact Information

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