

CWDM 10Gb/s SFP Optical Transceiver Module

SPP5100CP-GL-xx

(10GBASE-ER, 40km 1470nm to 1610nm Cooled EA-DFB-LD, PIN-PD)

Features

- ◆ 10Gb/s Serial Optical Interface
 - High quality and reliability optical device and sub-assemblies
 - Cooled EA-DFB laser for up to 40km over Single Mode Fiber
 - High sensitivity PIN photodiode and TIA
- ◆ SFP+ MSA Compliant
 - Easy supply management for hot pluggability
 - Duplex LC Receptacle
 - SFP Mechanical Interface for easy removal
 - SFI High Speed Electrical Interface
 - 2-wire interface for management and diagnostic monitor
 - Tx_Disable and Rx_LOS functions
- ◆ Protocol
 - IEEE802.3ae 10 Gigabit Ethernet
 - LAN PHY/WAN PHY
- ◆ Power Supply
 - Single 3.3V power supply
 - Low power consumption (max 2.0W)
- ◆ RoHS6 compliant

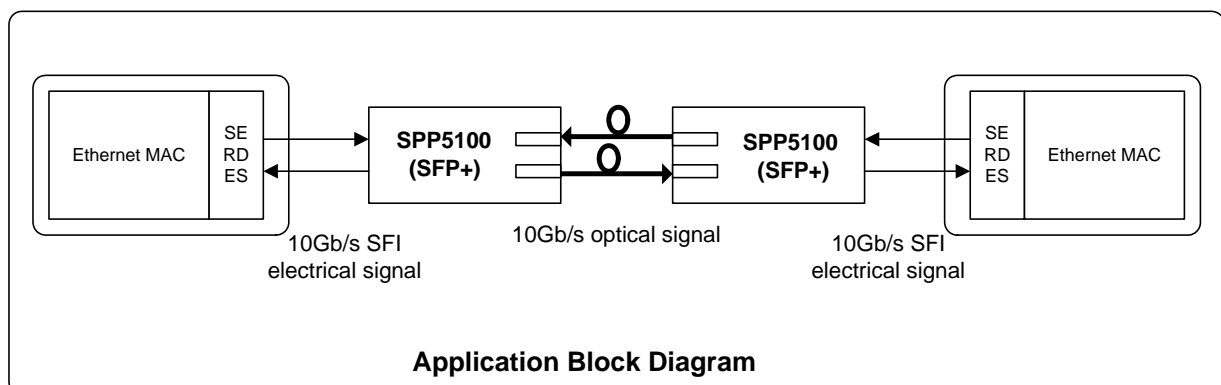


CWDM Specification

- 1470, 1490, 1510, 1530, 1550, 1570, 1590, 1610nm

Applications

- ◆ 10GE Ethernet switches and routers
- ◆ 10GE Storage
- ◆ Inter Rack Connection
- ◆ Other high speed data connections



1. General Description

The SPP5100CP-GL is a very compact 10Gb/s optical transceiver module for serial optical communication applications at 10Gb/s. The SPP5100CP-GL converts a 10Gb/s serial electrical data stream to 10Gb/s optical output signal and a 10Gb/s optical input signal to 10Gb/s serial electrical data streams. The high speed 10Gb/s electrical interface is fully compliant with SFI specification.

The SPP5100CP-GL is designed for Ethernet LAN (10.3Gb/s) and WAN(9.95Gb/s) applications. The high performance cooled EA-DFB-LD transmitter and high sensitivity PIN receiver provide superior performance for Ethernet applications at up to 40km links.

The fully SFP compliant form factor provides hot pluggability, easy optical port upgrades and low EMI emission.

Table 1. Fiber compliance

SFP+ type	Wavelength [nm]	Cable Type	Core Size (micron)	Modal Bandwidth [MHz/km]	Cable distance
10GB-ER	1470-1610	SMF	G.652	--	40km(Note1)

Note1. 40km transmission to represents 800ps/nm at 1611nm.

2. Functional Description

The SPP5100CP-GL contains a duplex LC connector for the optical interface and a 20-pin connector for the electrical interface. Figure 2.1 shows the functional block diagram of SPP5100CP-GL SFP Transceiver.

Transmitter Operation

The transceiver module receives 10Gb/s electrical data and transmits the data as an optical signal.

The transmitter output can be turned off by Tx disable signal, TX_DIS pin. When TX_DIS is asserted High, Transmitter is turned off.

Receiver Operation

The received optical signal is converted to serial electrical data signal.

The RX_LOS signal indicates insufficient optical power for reliable signal reception at the receiver.

Management Interface

A 2-wire interface (SCL, SDA) is used for serial ID, digital diagnostics and other control /monitor functions.

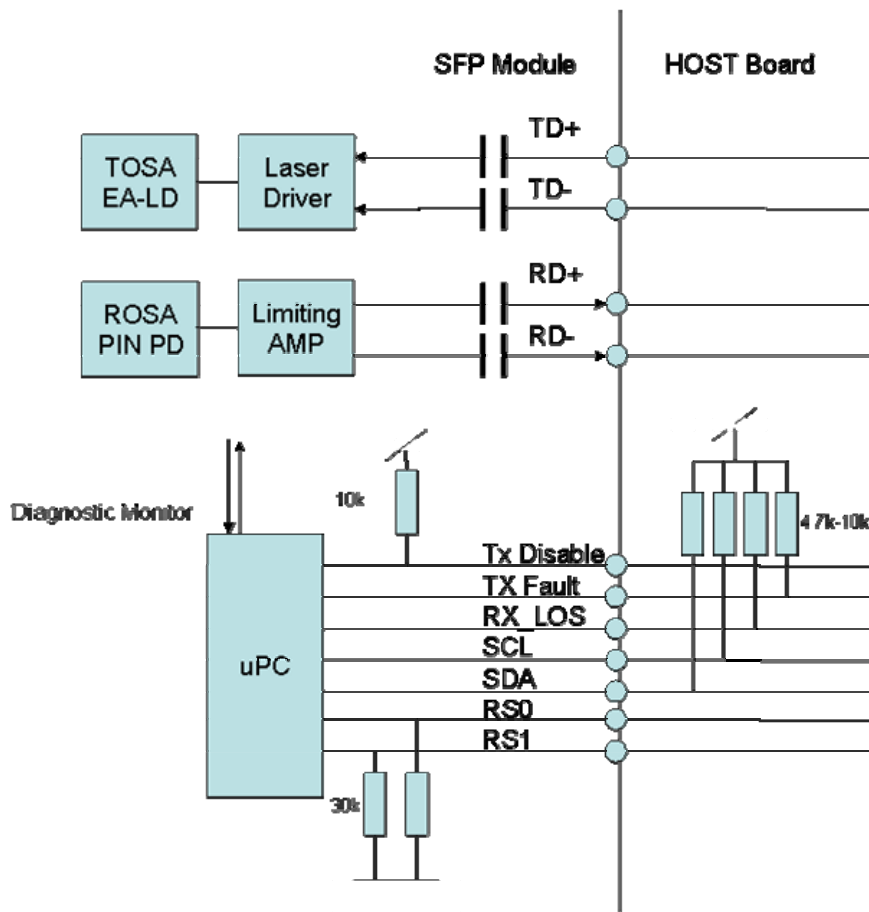


Figure 2.1. Functional Block Diagram

Package Dimensions

Figure 3.1. shows the package dimensions of SPP5100CP-GL. SPP5100CP-GL is designed to be compliant with SFP MSA specification. Package dimensions are specified in SFF-8432. (Note : Drawing below will be revised in the future./Bail color :RED)

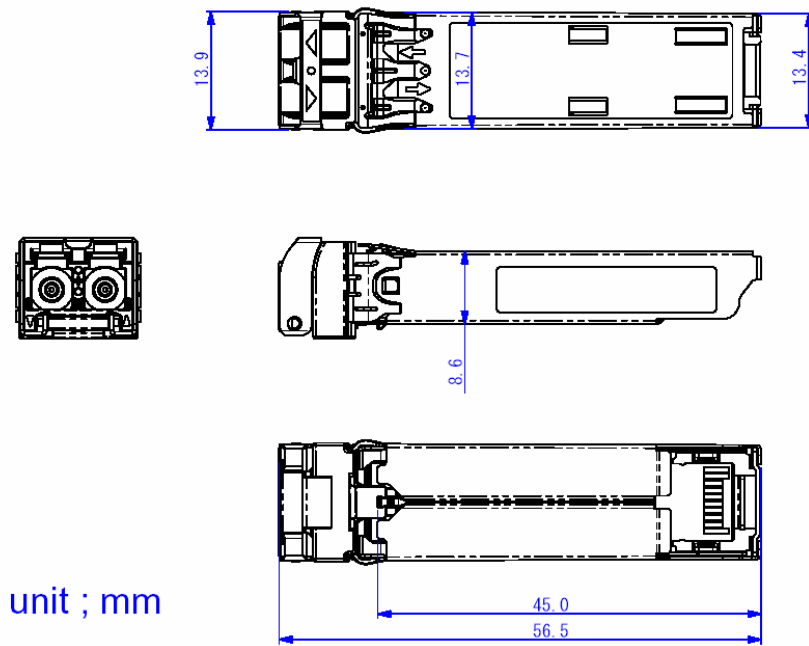


Figure 3.1. Package dimensions

3. Pin Assignment and Pin Description

3.1. SFP Transceiver Electrical Pad Layout

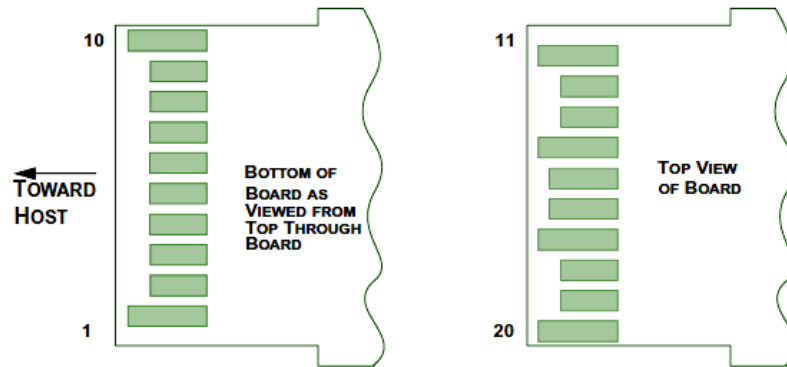


Figure 4.1. SFP Transceiver Electrical Pad Layout

3.2. Host PCB SFP Pinout

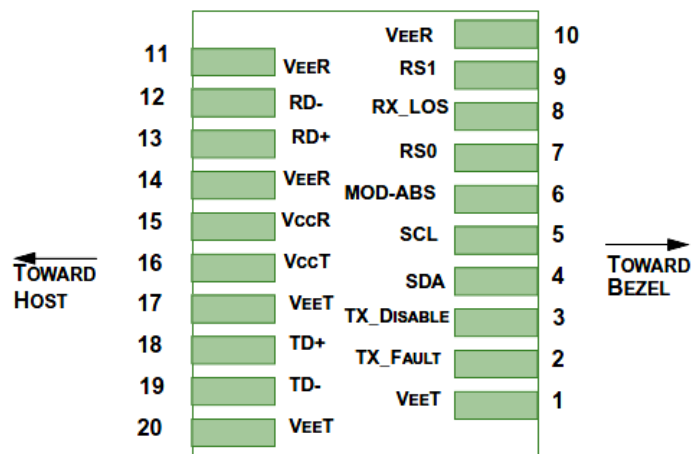


Figure 4.2. Host PCB SFP Pinout

3.3. Pin Descriptions

Table 4.3. Pin Description

Pin#	Name	Logic	Description	Power Sequence Order	Note
1	VeeT		Module Transmitter Ground	1 st	1
2	Tx_Fault	LVTTL-O	Module Transmitter Fault	3 rd	2
3	Tx_Disable	LVTTL-I	Transmitter Disable, Turns off transmitter laser output	3 rd	3
4	SDA	LVTTL-I/O	2 Wire Serial Interface Data Line (Same as MOD-DEF2 as defined in the INF-8074i)	3 rd	
5	SCL	LVTTL-I/O	2 Wire Serial Interface Data Line (Same as MOD-DEF1 as defined in the INF-8074i)	3 rd	
6	MOD_ABS		Module Absent, connected to VeeT or VeeR in the module	3 rd	2
7	RS0	LVTTL-I	Rate Select 0 (not functional for 10GE type)	3 rd	
8	RX_LOS	LVTTL-O	Receiver Loss of Signal Indication	3 rd	2
9	RS1	LVTTL-I	Rate Select 1 (not functional for 10GE type)	3 rd	
10	VeeR		Module Receiver Ground	1 st	1
11	VeeR		Module Receiver Ground	1 st	1
12	RD-	CML-O	Receiver Inverted Data Output	3 rd	
13	RD+	CML-O	Receiver Non-Inverted Data Output	3 rd	
14	VeeR		Module Receiver Ground	1 st	1
15	VccR		Module Receiver 3.3V Supply	2 nd	
16	VccT		Module Transmitter 3.3V Supply	2 nd	
17	VeeT		Module Transmitter Ground	1 st	1
18	TD+	CML-I	Transmitter Non-Inverted Data Input	3 rd	
19	TD-	CML-I	Transmitter Inverted Data Input	3 rd	
20	VeeT		Module Transmitter Ground	1 st	1

Note

- 1: Module ground pins are isolated from the module case and chassis ground within the module.
- 2: Shall be pulled up with 4.7k to 10k ohm to a voltage between 3.15V and 3.45V on the host board.
- 3: Shall be pulled up with 4.7k to 10k ohm to VccT in the module.

4. Absolute Maximum Ratings and Recommended Operating Conditions

Table 5.1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-40	85	degC	
Relative Humidity (non-condensation)	RH	-	85	%	
Operating Case Temperature	Topc	0	70	degC	
Supply Voltage	VccR/VccT	-0.5	3.6	V	
Voltage on LVTTL Input	Vilvttl	-0.5	VCC3+0.5	V	
LVTTL Output Current	Iolvttl	-	15	mA	
Voltage on Open Collector Output	Voco	0	6	V	
Receiver Input Optical Power(Average)	Mip	-	4	dBm	

Table 5.2. Recommended Operating Conditions and Supply Requirements

Parameter	Symbol	Min	Max	Unit	Note
Operating Case Temperature	Topc	0	70	degC	
Relative Humidity(non-condensing)	Rhop	-	85	%	
Power Supply Voltage	VccR/VccT	3.135	3.465	V	
Total Power Consumption	Pd	-	2.0	W	1

Note:

1: The inrush current is MSA Compliant.

5. Electrical Interface

5.1. High Speed Electrical Interface

SFI Application Reference model

Figure 6.1.1. shows the high speed electrical interface (SFI) compliance points.

SFI electrical interface is specified for each compliance point in the SFP MSA specification.

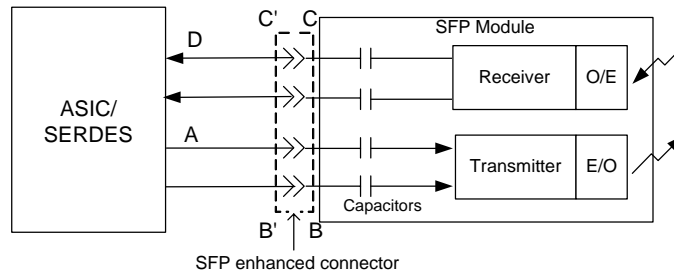


Figure 6.1.1. SFI Application Reference Model

SFI Module Transmitter Input Electrical Interface Specification at B' and Calibrated B''

Table 6.1.1. SFI Transmitter Input Electrical Specification at B'

Parameter B'	Symbol	Condition	Min	Typ.	Max.	Unit
Single Ended Output Voltage Tolerance		Referenced to VeeT	-0.3		4.0	V
AC common Input S-parameter		Note 1	15			mV
Differential Input S-parameter (note 1)	SDD11	0.01-4.1GHz			Note 2	dB
		4.1-11.1GHz			Note 3	dB
Reflected Differential to Common Mode Conversion	SCD11	0.01-11.1GHz			-10	dB

Note 1. Measured at B'' with Host Compliance Board and Module Compliance Board pair.

2. Maximum Reflection Coefficient given by equation $SDD11(dB) = -12 + 2 * \sqrt{f}$, with f in GHz.

3. Maximum Reflection Coefficient given by equation $SDD11(dB) = -6.3 + 13 \log_{10}(f/5.5)$, with f in GHz

Table 6.1.2. SFI Transmitter Input Electrical Specification at B"

Parameter B"	Symbol	Condition	Min	Typ.	Max.	Unit
Crosstalk Source Rise/Fall time (20% to 80%)	Tr, Tf	Note 1, 2		34		ps
Crosstalk Source Amplitude (p-p differential)		Note 1, 2		1000		mV
AC Common Mode Voltage		Note 3			15	mV(RMS)
Total Jitter	TJ				0.28	UIpp
Data Dependent Jitter	DDJ			0.10		UIpp
Pulse Width Shrinkage Jitter	DDPWS			0.055		UIpp
Uncorrelated Jitter	UJ	Note 4		0.023		UIrms
Eye Mask Figure 6.1.2	X1			0.12		UI
	X2			0.33		UI
	Y1			95		mV
	Y2			350		mV

- Note 1. Measured at C" with Host Compliance Board and Module Compliance Board pair.
2. Since the minimum module output transition time is faster than the crosstalk transition time the amplitude of crosstalk source is increased to achieve the same slew rate.
3. The tester is not expected to generate this common mode voltage however its output must not exceed this value.
4. It is not possible to have the worst UJ and DDJ simultaneously and meet the TJ specifications if the UJ is all Gaussian.

SFI Module Receiver Output Electrical Interface Specification at C'

Table 6.1.3. SFI Receiver Output Electrical Specification at C'

Parameter – C'	Symbol	Conditions	Min	Typ	Max	Units
Crosstalk source rise/fall time (20% to 80%)	Tr, Tf	Note 1		34		ps
Crosstalk Source Amplitude Differential (p-p)		Note 2		700		mV
Termination Mismatch at 1 MHz	ΔZ_M				5	%
Single Ended Output Voltage Tolerance			-0.3		4.0	V
Output AC Common Mode Voltage					7.5	mV (RMS)
Differential Output S-parameter (Note 3)	SDD22	0.01-4.1GHz			Note 2	dB
		4.1-11.1GHz			Note 3	dB
Common Mode Output Reflection Coefficient (Note 5)	SCC22	0.01-2.5GHz			Note 4	dB
		2.5-11.1GHz			-3	dB

Note 1 : Measured at B" with the Host Compliance Board and Module Compliance Board pair.

2 : Reflection Coefficient given by equation $SDD22(dB) < -12 + 2 \times \text{SQRT}(f)$, with f in GHz.

3 : Reflection Coefficient given by equation $SDD22(dB) < -6.3 + 13 \times \log_{10}(f/5.5)$, with f in GHz.

4 : Reflection coefficient given by equation $SCC22(dB) < -7 + 1.6 \times f$, with f in GHz.

Table 6.1.4. SFP+ Limiting Output Jitter and Eye Mask Specification at C'

Parameter – C'	Symbol	Conditions	Min	Typ	Max	Units
Output rise/fall time (20% to 80%)	Tr, Tf		28			ps
Total Jitter	TJ				0.70	UIpp
99% Jitter	J2	Note 1			0.42	UIpp
Eye Mask Figure 6.1.3	X1		0.35			UI
	Y1		150			mV
	Y2		425			mV

Note 1 : J2 is defined from the 0.5th to the 99.5th percentile of the jitter histogram..

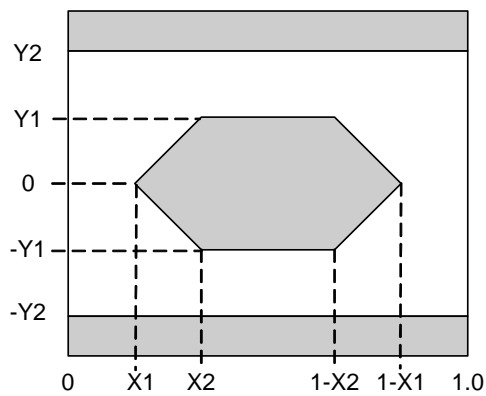


Figure 6.1.2.
Transmitter Input Eye Mask

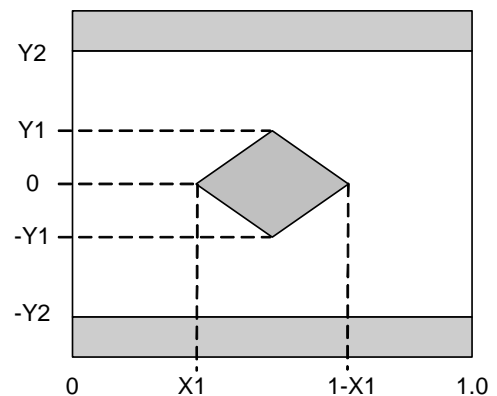


Figure 6.1.3.
Receiver Output Eye Mask

5.2. Low speed Electrical Interface

SPP5100CP-GL low speed interface is based on 2-wire interface. Management memory map is based on SFF-8472.

2-wire Electrical Specifications

Parameter	Symbol	Min	Max	Unit
Host 2-wire Vcc	Vcc_host	3.14	3.46	V
SCL and SDA	V _{OL}	0.0	0.40	V
	V _{OH}	Vcc_host-0.5	Vcc_host+0.3	V
SCL and SDA	V _{IL}	-0.3	VccT*0.3	V
	V _{IH}	VccT*0.7	VccT+0.5	V
Input current on the SCL and SDA contacts		-10	10	uA
Capacitance on SCL and SDA I/O contact			14	pF

2-wire Timing Specifications

Parameter	Symbol	Min	Max	Unit
Clock Frequency	f _{SCL}	0	400	kHz
Clock Pulse Width Low	t _{LOW}	1.3		us
Clock Pulse Width High	t _{HIGH}	0.6		us
Time bus free before new transmission can start	t _{BUF}	20		us
START Hold Time	t _{HD, STA}	0.6		us
START Set-up Time	t _{SU, STA}	0.6		us
Data In Hold Time	t _{HD, DAT}	0		us
Data In Set-up Time	t _{SU, DAT}	0.1		us
Input Rise Time (100kHz)	t _{r, 100}		1000	ns
Input Rise Time (400kHz)	t _{r, 400}		300	ns
Input Fall Time (100kHz)	t _{f, 100}		300	ns
Input Fall Time (400kHz)	t _{f, 400}		300	ns
STOP Set-up Time	t _{SU, STO}	0.6		us
Serial Interface Clock Holdoff “Clock Stretching”	t _{clock_hold}		500	us

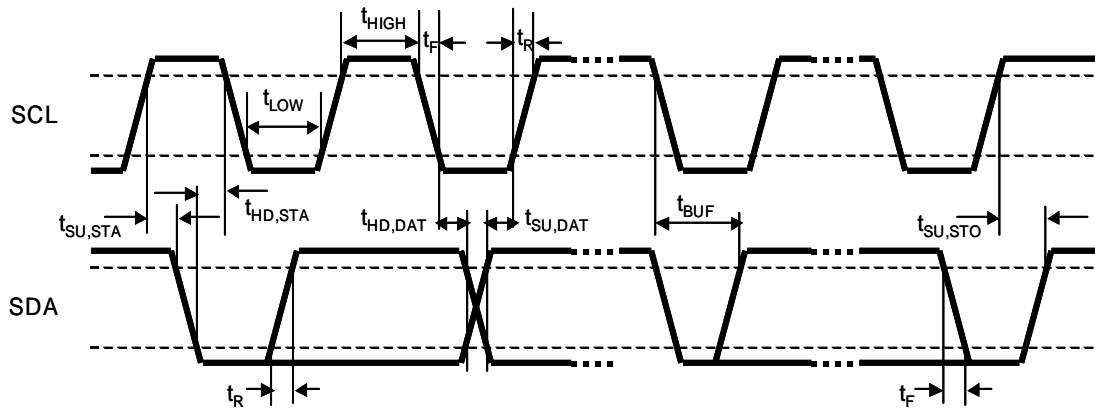


Figure 6.2.1 SFP+ Timing Diagram

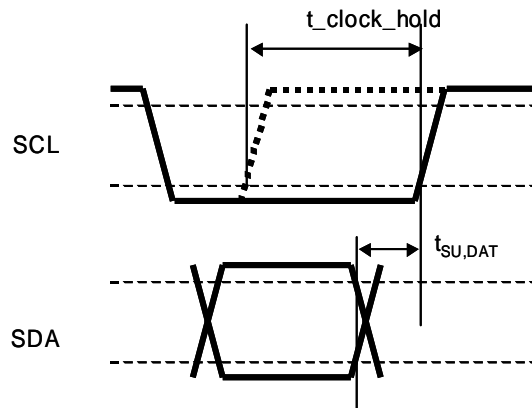


Figure 6.2.2. Detail of Clock Stretching

6. Optical Interface

Optical Interfaces of SPP5100CP-GL are defined in the IEEE802.3ae(10GBASE-ER).

Figure 7.1. Optical Transmitter

Parameter	Symbol	Min	Typ	Max	Unit
Signaling Speed (LAN PHY)		-	10.3125		Gb/s
(WAN PHY)			9.95328		
Signaling speed variation from nominal (max)		-100		+100	ppm
Center wavelength (Note 1)		1470		1610	nm
Spectral Width	dl	-		1	nm
Side Mode Suppression Ratio	SMSR	30			dB
Average launched power	Pave	-4.7		+4.0	dBm
OMA	Poma	-1.7			dBm
OMA-TDP		-2.1			dBm
Transmitter and dispersion penalty	DP			3.0	dB
Average launch power of Tx OFF	Pave_off			-30	dBm
Extinction ratio (Note 2)	ER	3.0			dB
RIN OMA	RIN			-128	dB/Hz
Optical Return Loss Tolerance	ORLT			21	dB
Eye mask(X1,X2,X3,Y1,Y2,Y3)		(0.25, 0.40, 0.45, 0.25, 0.28, 0.40) (Note 3)			

Note 1 : See Figure 7.2.

Note 2 : Dispersion is 800ps/nm at 1600nm.

Note 3 : Refer to Figure 7.1.

Figure 7.2. Wavelength Table

Part No.	Band	Min	Typ	Max	Unit
SPP5100CP-GL-47	S-band	1464.5	1471	1477.5	nm
SPP5100CP-GL-49	S-band	1484.5	1491	1497.5	nm
SPP5100CP-GL-51	S-band	1504.5	1511	1517.5	nm
SPP5100CP-GL-53	C-band	1524.5	1531	1537.5	nm
SPP5100CP-GL-55	C-band	1544.5	1551	1557.5	nm
SPP5100CP-GL-57	L-band	1564.5	1571	1577.5	nm
SPP5100CP-GL-59	L-band	1584.5	1591	1597.5	nm
SPP5100CP-GL-61	L-band	1604.5	1611	1617.5	nm

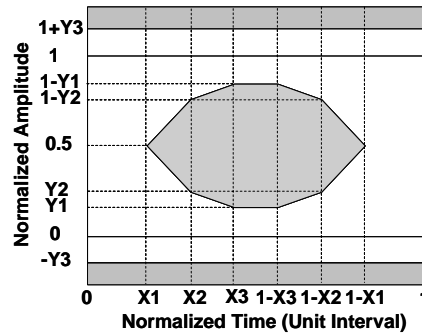


Figure.7.1. Transmission eye mask definition

Optical Receiver

Parameter	Symbol	Min	Typ	Max	Unit
Wavelength		1460		1620	nm
Signaling Speed (LAN PHY)			10.3125		Gb/s
(WAN PHY)			9.95328		
Signaling speed variation from nominal (max)		-100		+100	ppm
Average receiver power (Note 1)		-15.8		-1.0	dBm
Receiver sensitivity in OMA				-14.1	dBm
Receiver Reflectance				-26	dB
Stressed receiver sensitivity in OMA (Note 2)				-11.3	dBm
Vertical eye closure penalty		2.7			dB
Stressed ey jitter		0.3			UIpp
Receive electrical 3dB upper cutoff frequency				12.3	GHz

Note 1 : Receiver sensitivity is informative. Stressed receiver sensitivity shall be measured with conformance test signal for BER=10⁻¹².

Note 2 : The stressed sensitivity value in the table are for system level BER measurements which include the effects of CDR circuit.

8. Electrical and Optical I/O Signal Relationship

Table.8.1. TX_DIS vs. Optical Output Power

TX_DIS	Optical Output Power
Low ($V_{IL} = -0.3$ to $0.8V$)	Enabled
High ($V_{IH} = 2.0$ to $VCC3+0.3V$)	Disabled ($< -30dBm$)

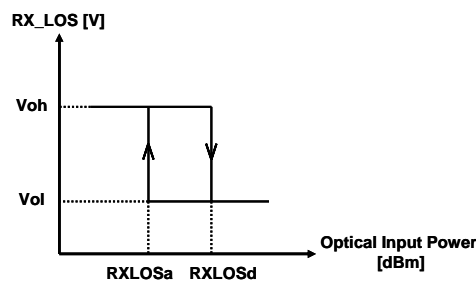


Figure.8.1. Optical Input Power vs. RX_LOS

9. User Interface

9.1. SFP Mechanical Interface

SFP Mechanical Interface is specified in the SFF-8432. Also, bail latch system is adequate for the particular specification.

9.2. Management Interface

SFP 2-Wire Serial Interface Protocol

SFP 2-wire serial interface is specified in the SFF-8472.

The SFP 2-wire serial interface is used for serial ID, digital diagnostics, and certain control functions. The 2-wire serial interface is mandatory for all SFP modules.

The 2-wire serial interface address of the SFP module is A0h and A2h. In order to access to a specific module on the 2-wire serial bus, the SFP has a MOD_ABS (module absent pin). This pin, which is pulled down in the module, must be held low to notify a module installation and to allow communication over 2-wire serial interface.

SFP Management Interface

SFP Managed interface is specified in the SFF-8472.

The Figure 9.2. shows the structure of the memory map. The normal 256 Byte address space is divided into lower and upper blocks of 128 Bytes. The lower block of 128 Byte is always directly available and is used for the diagnostics and control functions that must be accessed repeatedly.

Multiple blocks of memories are available in the upper 128 Bytes of the address space. These are individually addressed through a table select Byte which the user enters into a location in the lower address space. The upper address space tables are used for less frequently accessed functions and control space for future standards definition.

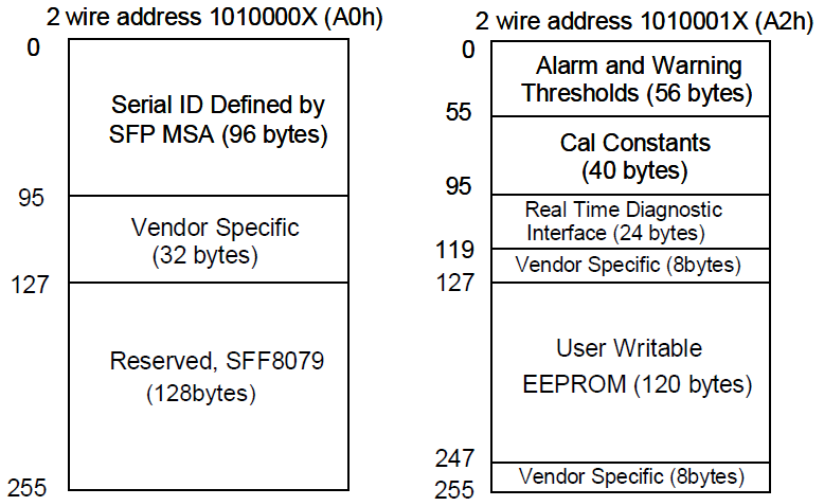


Figure 9.1. 2-wire Serial Interface Memory Map

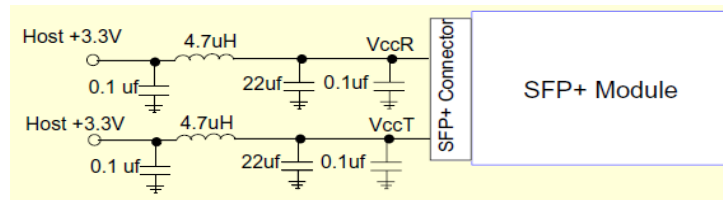


Figure 9.2. Supply Filter

9.3. Serial ID Memory Map (Data Field – Address A0h)

Address	Size (Bytes)	Name	Hex	ASC	Description
0	1	Identifier	03		SFP module
1	1	Ext.Identifier	04		Serial ID module
2	1	Connector	07		LC Connector
3			80		Unallocated
4			00		
5			00		
6	8	Transceiver	00		
7			00		
8			00		
9			00		
10			00		
11	1	Encoding	06		64B66B
12	1	BR, Nominal	67		10.3Gbps
13	1	Rate Identifier	00		unspecified
14	1	Length(9um, km)	28		40km
15	1	Length(9um)	FF		> 25.5km
16	1	Length(50um)	00		not support MMF
17	1	Length(62.5um)	00		not support MMF
18	1	Length(Copper)	00		not support copper
19	1	Length(OM3)	00		not support MMF
20			53	S	
21			75	u	
22			6D	m	
23			69	i	
24			74	t	
25			6F	o	
26			6D	m	
27			6F	o	
28			45	E	
29			6C	l	
30			65	e	
31			63	c	
32			74	t	
33			72	r	
34			69	i	
35			63	c	
36	1	Channel Spacing	00		
37			00		
38	3	Vendor OUI	00		
39			5F		
40			53	S	
41		50	P		
42		50	P		
43		35	5		
44		31	1		
45		30	0		
46		30	0		
47		43	C		
48		50	P		
49		2D	-		
50		47	G		
51		4C	L		
52		2D	-		
53			x		*4
54			x		
55			20		
56			41	A	*1
57			20		
58			20		
59			20		
60				x	
61	2	Wavelength		x	*4
62	1				
63	1	CC_BASE	xx		Check Code *2

Address	Size (Bytes)	Name	Hex	ASC	Description		
64	2	Options	04		Unspecified		
65			1A	limit Receiver Output TxDisable, TxFault, LOS implemented			
66	1	BR,max	00				
67	1	BR,min	00				
68			xx				
69			xx				
70			xx				
71			xx				
72			xx				
73			xx				
74			xx				
75	16	Verdor SN	xx				
76			xx				
77			xx				
78			xx				
79			20				
80			20				
81			20				
82			20				
83			20				
84					xx		
85					xx		Year code
86					xx		
87					xx		Month code
88					xx		
89					xx		Day code
90					xx		
91			xx		LOT code		
92	1	Diagnosis Monitoring Type	68		Internal cal, Average Power Alarm/Warning flags, Soft TxDisable, Soft TxFault, Soft RxLOS implemented		
93	1	Enhanced Options	F0				
94	1	SFF-8472 Compliance	04		Rev.10.4		
95	1	CC_EXT	xx		Check Code *3		
96-126	32	Vendor Specific	xx				
127-255	125	Reserved	00				

*1 : Revision level for part number provided by vendor (ASCII). Variable
 *2 : Checksum of Add.0 to 62
 *3 : Checksum of Add.64 to 94

Wavelength	Code (xx)
1471nm	47
1491nm	49
1511nm	51
1531nm	53
1551nm	55
1571nm	57
1591nm	59
1611nm	61

9.4. Alarm/Warming threshold

A2h address	Meaning	Unit	SPP5100CP-GL-xx
0-1	Temperature High Alarm	deg	85
2-3	Temperature Low Alarm	deg	-15
4-5	Temperature High Warning	deg	80
6-7	Temperature Low Warning	deg	-10
8-9	Voltage High Alarm	V	3.63
10-11	Voltage Low Alarm	V	3.00
12-13	Voltage High Warning	V	3.55
14-15	Voltage Low Warning	V	3.10
16-17	Tx Bias High Alarm	mA	97.5
18-19	Tx Bias Low Alarm	mA	22.5
20-21	Tx Bias High Warning	mA	91.0
22-23	Tx Bias Low Warning	mA	27.0
24-25	Tx Power High Alarm	dBm	5.5
26-27	Tx Power Low Alarm	dBm	-6.5
28-29	Tx Power High Warning	dBm	4.0
30-31	Tx Power Low Warning	dBm	-5.0
32-33	Rx Power High Alarm	dBm	1.0
34-35	Rx Power Low Alarm	dBm	-17.8
36-37	Rx Power High Warning	dBm	-1.0
38-39	Rx Power Low Warning	dBm	-15.8

Note. Alarm /Warming flag is linked to TxFault by default setting.

9.5. Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

Parameter	Accuracy	Unit
Internally measured transceiver temperature	+/- 3	deg.C
Internally measured transceiver supply voltage	+/- 3	%
Measured Tx bias current	+/- 10	%
Measured Tx output power	+/- 2	dB
Measured Rx received average optical power	+/- 3	dB

10. RoHS COMPLIANCY

Compliance versus requirements contained inside the following reference document is guaranteed: "Directive 2002/95/EC of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment" from official journal of European Union (European Parliament and of the Council). This product is Compliant at RoHS-6/6 level and contains no leaded solders.

11. Qualification Testing

SPP5100CP-GL 10Gb/s transceiver is qualified to Sumitomo Electric Industries internal design and manufacturing standards. Telecordia GR-468-CORE reliability test standards, using methods per MIL-STD-883 for mechanical integrity, endurance, moisture, flammability and ESD thresholds, are followed.

12. Laser Safety Information

SPP5100CP-GL transceiver uses a semiconductor laser system that is classified as Class 1 laser products per the Laser Safety requirements of FDA/CDRH, 21 CFR1040.10 and 1040.11. These products have also been tested and certified as Class 1 laser products per IEC 60825-1:2007 and IEC60825-1:2001 and EN60825-1:2007 standards.

Caution

If this product is used under conditions not recommended in the specification or is used with unauthorized revision, the classification for laser product safety is invalid. Reclassify the product at your responsibility and take appropriate safety measures.

13. Electromagnetic Compatibility

EMI (Emission)

SPP5100CP-GL is designed to meet FCC Class B limits for emissions and noise immunity per CENELEC EN50 081 and 082 specifications.

RF Immunity

SPP5100CP-GL has an immunity to operate when tested in accordance with IEC 61000-4-3 (80- 1000MHz, Test Level 3) and GR-1089.

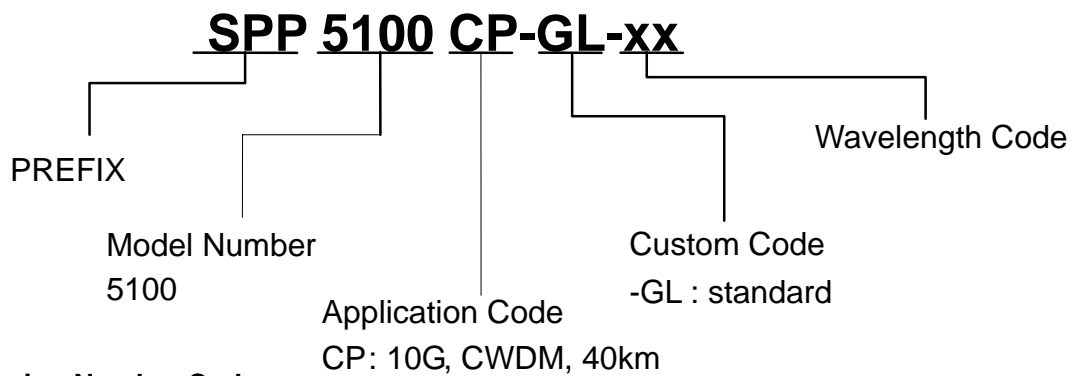
Electrostatic Discharge (ESD) Immunity

SPP5100CP-GL has an immunity against direct and indirect ESD when tested accordance with IEC 61000-4-2.

14. Firmware version

15. Ordering Information

15.1. Part Numbering System



15.2. Ordering Number Code

Table 15-1. SPP5100CP Application Code

part Number	Temperature Range	Distance	Fiber	E/O	O/E	Telcordia GR-253	ITU-T	IEEE 802.3	ANSI
SPP5100ER-GL	0 to 70 deg.C	40km	SMF	Cooled EA-DFB 1550nm	PIN	-	-	10GBASE-ER	-

Wavelength	Code (xx)
1471 nm	47
1491 nm	49
1511 nm	51
1531 nm	53
1551 nm	55
1571 nm	57
1591 nm	59
1611 nm	61

15. Label information (Top label)



16. Contact Information

U.S.A.

Sumitomo Electric Device Innovations, U.S.A., Inc.

<West Coast (USA Headquarters)>

2355 Zanker Rd. San Jose, CA 95131-1138, USA

Tel: +1-408-232-9500

Fax: +1-408-428-9111

<East Coast>

4021 Stirrup Creek Drive, Suite 200, Durham, NC 27703, USA

Tel: +1-919-361-1600

Fax: +1-919-361-1619

Email: information@sei-device.com

<http://www.sei-device.com/>

Europe

Sumitomo Electric Europe Ltd.

220 Centennial Park, Elstree, Herts, WD6 3SL UK

Tel: +44-208-953-8681

Fax: +44-208-207-5950

E-mail: photonics@sumielectric.com

<http://www.sumielectric.com>

Asia

Sumitomo Electric Asia Ltd.

Photonics Department

Room 2624 - 2637, 26F., Sun Hung Kai Center, 30 Harbour Road, Wanchai, Hongkong.

Tel: +852-2576-0080

Fax: +852-2576-6412

Japan

Sumitomo Electric Industries, Ltd.

Device Sales Department

<Tokyo>

3-9-1, Shibaura, Minato-ku, Tokyo 108-8539, Japan

TEL +81-3-6722-3286

FAX +81-3-6722-3284

<Osaka>

4-5-33, Kitahama, Chuo-ku, Osaka 541-0041, Japan

Tel: +81-6-6220-4245

Fax: +81-6-6222-6231

E-mail: optoele-sales-pro-sml@list.sei.jp

<http://www.sei.co.jp/products/index.html>